REMARKS

The present response is to the Office Action mailed in the above-referenced case on May 22, 2003. Claims 1-42 are pending for examination. Claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34 and 36-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemirovsky (DISC, A Dynamic Stream Computer), hereinafter Nemirovsky. Claims 4, 13-14, 18, 27-28, 32 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky as applied to claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34 and 36-40, and further in view of Nemirovsky et al. (DISC, A Dynamic Stream Computer), hereinafter Nemirovsky et al. Claims 7, 21 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky as applied to claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34 and 36-40, and further in view of applicant's admission.

Applicant has again carefully studied the prior art presented by the Examiner, and the Examiner's rejections and statements in the instant Office Action. In response, applicant herein amends the base claims to more particularly point out and distinctly claim the subject matter of applicant's invention regarded as patentable. Applicant herein presents further argument to more particularly point out the key and patentable distinction of applicant's invention as recited in the base claims as amended, and to establish that the claims as amended are now clearly and unarguably patentable over the prior art reference.

Applicant herein amends the language of claim 1 to specifically recite a multistreaming processor system comprising a plurality of physical hardware streams for streaming one or more instruction threads, and at the time of detection of interrupts or exceptions, a specific physical stream is directed to process the specific interrupt or exception. Applicant reproduces claim 1 as amended below.

Applicant's claim 1 as amended now recites:

1. (Currently Amended) A multi-streaming processor system comprising:

a plurality of physical hardware streams for streaming one or more instruction threads;

a set of functional resources for processing instructions from streams; and interrupt logic;

wherein through the interrupt logic specific interrupts or exceptions are detected and at the time of their detection a specific stream of the plurality of physical hardware streams is directed to process the specific interrupt or exception.

Applicant's claims 15 and 29 recite a method for processing interrupts in a multi-stream processor and a computer system for practicing the invention in accordance with applicant's claim 1, and are herein similarly amended in the present response.

In the previous response filed by applicant on April 17, 2003, applicant argued that detection of interrupts or exceptions, and directing a specific stream or streams to process specific detected interrupts or exceptions, at the time of detection, is a key and important limitation of applicant's invention which deserves patentable weight, and that the teachings of Nemirovsky cannot read on applicant's claims as amended in the previous response, because Nemirovsky teaches assigning two out of four streams concurrently to interrupts, teaching away from directing a specific stream to process a specific interrupts or exception at the time of detection. Nemirovsky, therefore, teaches an alternative system and method which accomplishes a similar but different purpose then applicant's invention, and clearly fails to anticipate all of the limitations of applicant's claims as amended.

The Examiner has kindly provided a response in the instant Office Action, to applicant's previous argument and amendments, stating that Nemirovsky

expressly teaches that the interrupt can directly activate an instruction stream and that an interrupt can create its own instruction stream, and activation of the instruction stream would be in response to the detection, as it is taught that the interrupt routine is finished, and the throughput is dynamically reallocated. The Examiner stated further that Nemirovsky teaches that the instruction streams are dynamically assigned, and the reference teaches that in response to an interrupt a stream is created, and the stream would be directed to process the interrupt.

Applicant agrees that Nemirovsky teaches that the instruction streams are dynamically assigned and a stream is created to process the interrupt or exception. It has only now become clear to the applicant that Examiner is treating the Nemerovsky reference as though it is a processor having physical hardware streams. The patentable distinction of applicant's invention has now finally come into focus. The dynamic instruction stream computer (DISC) of Nemirovsky is not a hardware implemented or "physical" multistreaming processor, as taught in applicant's invention and recited in applicant's base claims as amended; rather, Nemirovsky teaches a "virtual" multistreaming processor wherein virtual streams are created in a single-streaming processor by instruction interleaving. Because the streams are software dependent in the reference, almost anything can be done; but the reference cannot read on operations in a processor having a physical plurality of streams. Applicant now understands the reason for the Examiner's previous statements pertaining to the distinctions between applicant's invention and that Nemirovsky.

Applicant now wishes to direct the Examiner's attention to page 80 of the reference of Nemirovsky, specifically the portion entitled "Multiple Instruction Streams", which discloses that every instruction stream of the multiple instruction streams running on the dynamic instruction stream computer can be called a "virtual processor", accomplished by having the context of four instruction streams in the processor. The scheduler then fetches one instruction per cycle, and the instructions can be selected from any one of the "virtual processors". The Abstract of the Nemerovsky reference is also instructional in this respect, stating

that "The DISC operates by allowing multiple instruction streams (ISs), representing different processes to run concurrently by instruction interleaving on the pipeline." (emphasis added) There is a single pipeline as opposed to multiple pipelines of a true (hardware) multistreaming processor, as in the present invention.

The multistreaming processor taught in applicant's invention, and now recited in applicant's base claims as amended, comprises physical or "real" instruction streams, not" virtual" streams created by Interleaving, as taught in Nemirovsky. Applicant's invention teaches that the instruction stream is a hardware capability for supporting/processing an instruction thread running within the stream.

With physical streams it is necessary in the prior art to have a stream preassigned to interrupts. Applicant's invention, however, teaches an improvement in interruption logic such that the interrupt logic is capable of selecting any stream to process an interrupt or exception, at the time the interrupt or exception is detected. The disclosure of Nemirovsky, therefore, clearly cannot read on applicant's claims as amended, because Nemirovsky does not disclose, suggest or intimate a multistreaming processor comprising multiple, physical instruction streams, as is taught in applicant's invention, and now recited in applicant's base claims as amended.

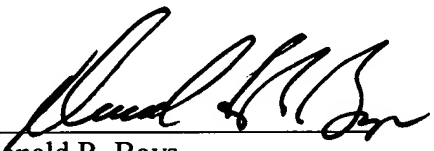
The key limitations in applicant's claims as amended now clearly and unarguably distinguish applicant's invention over that of Nemirovsky. Applicant therefore believes that independent claims 1, 15 and 29 as amended herein are now patentable over Nemirovsky. Depending claims to 2-14, 16-28 and 30-42 are then patentable on their own merits, or at least as depended from a patentable claim.

The Examiner has rejected claims 4, 13-14, 18, 27-28, 32 and 41-42 as being unpatentable over Nemirovsky as applied to claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, and 36-40, and further in view of Nemirovsky et al. In view of applicant's amendments to the base claims and further argument presented

above on behalf of the amended claims, the above depending claims are patentable on their own merits, or at least as depended from a patentable claim, as Nemirovsky now clearly and unarguably fails to anticipate all of the specific limitations of applicant base claims as amended and argued above.

As all of the claims standing for examination as amended have been shown to be patentable over the art of record, applicant respectfully requests reconsideration and that the present case be passed quickly to issue. If there are any time extensions needed beyond any extension specifically requested with this amendment, such extension of time is hereby requested. If there are any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted
Mario D. Nemirovsky et al.

by 
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